Remarks

In the Office action mailed 8/23/2005, claims 1-8 and 10 were rejected. Claim 9 was objected to.

In paragraph 4 of the Office action, claims 1, 6 and 10 were rejected under 35 U.S.C. 102(b) as being anticipated by Campardo et al. (U.S. Pat. No. 5,535,157). Campardo teaches one time programmable (OTP) memory cells in a row within a memory array plus other rows of EEPROM cells. But the memory transistors of Campardo are all shown to be EEPROMs in Fig. 1 with special voltages applied. One time programming (OTP) is achieved by placing a special voltage on the row decode line to prevent erasing. (See Campardo's specification, col. 3, lines 3-8 and claim 6). Therefore, all of the transistors are the same in Campardo.

On the other hand, some of Applicant's memory cells are mask programmed (ROM) while other memory cells are user programmed (non-volatile or EEPROM). This would normally give rise to different areawise footprints because mask programming implies that special masks are used for programming that give rise to different transistor geometries. The idea that diverse memory cells have equal area (L x W) footprints is explained in the specification, for example, on page 5, lines 10-13 and lines 34-46, for the ROM cells, as well as lines 1-3 for the EEPROM cells. Applicant has amended the independent claims to set out the mask programmed nature of the ROM transistors (see specification, page 2, lines 9-10 and Figs. 3-6) and the user programmable nature of the non-volatile transistors (Figs. 1 and 2). Both of these diverse types of transistors have the same area (L x W) or areawise footprint. This is not shown in the prior art and is believed to be patentable. The prior art cannot anticipate this because the prior art does not show both user programmable and mask programmed transistors having the same areawise footprint.

In paragraph 7 of the Office action, claims 2 and 3 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashikoshi et al. ('928) over Campardo et al. ('157). The Office action asserts that Fig. 5 and the Abstract of Hayashikoshi disclose memory cells with the same footprint. Applicant objects to this statement. No areawise footprints are shown in the reference. See remarks above. Campardo et al. does not supply the missing claimed subject matter.

Both claims 2 and 3 include all of the limitations of claim 1. The common electrode teaching shown on page 6 of the Office action has no bearing on the misssing footprint information. The rejection is believed to be traversed.

In paragraph 8 of the Office action, claims 4 and 5 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Campardo and Hayashikoshi or Campardo and Ho, respectively. Claims 4 and 5 include all of the limitations of claim 1, particularly the "same footprint" for the diverse memory cells, a feature not found in the prior art. The same remarks are applicable to paragraph 9 of the Office action regarding claims 7 and 8.

Summary and Conclusion

Applicant appreciates the indication of patentable subject matter in claim 9. Additional claims 20-30 have been added relating to the mask programmability of the ROM transistors to different logic states but having the same areawise footprint.

Reconsideration of the claims is requested in view of the amendment of the claims and remarks herein. A notice of allowance is respectfully solicited.

Respectfully submitted,

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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